Efficient Implementation of 5G Baseband Kernels on a Vector Processor

Vodafone Chair – Synopsys Cooperation

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Background / Objectives:

The impact of disruptive changes that the fifth generation (5G) era is bringing in the fields of industrial automation, vehicle communications and autonomous driving, IoT, health care, agriculture and massive mobile broadband transmission is significant. It is certain that 5G opens and creates new markets with limitless possibilities for growth and establishment as a new generation market leader.

In this project a PhD student from Technical University Dresden (TUD) cooperates with Synopsys on the development of a vector processor for high-performance baseband processing and associated software. The motivation for establishing the project is to enhance the institutional knowledge within the Company's R&D product development team for a potential "ARC communications DSP" for 5G terminal processing and other potential applications.

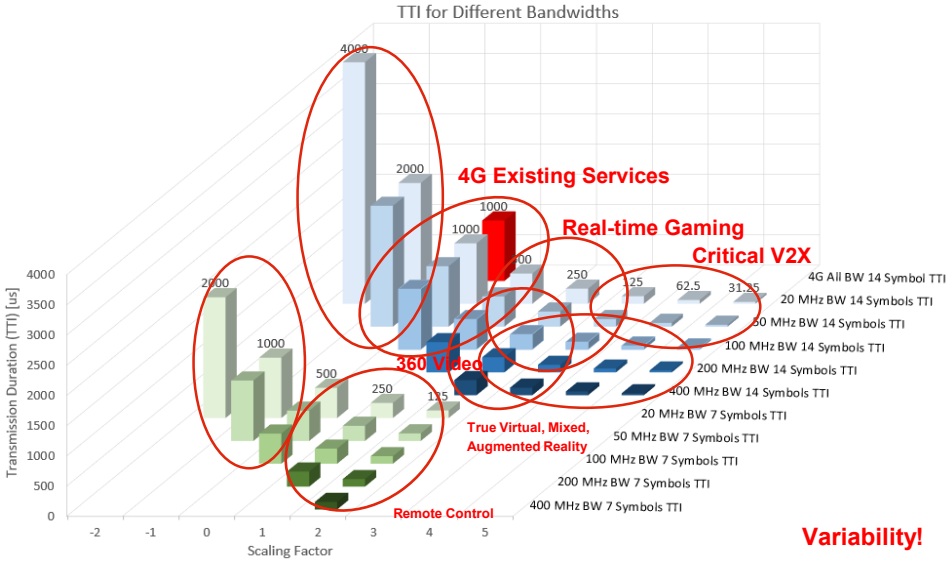
Approach:

This project consists of the following activities:

- Identify and study key 5G baseband kernels of terminal
- Identify and study key algorithms that dominate processing workloads in 5G baseband processing. Understand complexity, precision requirements, data types, parameter ranges {e.g. matrix sizes), etc.
- Analyse data locality of vectors/matrices sent between kernels/tasks and define memory interface {bandwidth) requirements.
- Identify natural boundaries for multi-core partitioning of baseband processing.
- Analyze the dynamic range of processing requirements of different SG streams.
- Study efficient mappings of SG kernels onto vector processor
- Prototype benchmark code with associated test software for functional verification.
- Prototype memory interface requirements onto proposed hardware architectures.
- Optimize benchmark code for efficient implementation on prototype vector processor.
- Analyze memory addressing and define address generation requirements.
- Map low data-rate streams onto architecture and optimize for low-power operation.
- Explore architecture enhancements for improving efficiency of kernel implementations
- Propose ISA enhancements, evaluate memory subsystem, use of predication, scatter/gather, etc.
- Explore if big/little approach reasonable.
- Evaluate proposed architecture enhancements using (extensible) prototype of vector processor (initial fully functional prototype provided by Synopsys). Key metrics will be cycle efficiency and energy efficiency, but also other aspects like code size, impact on programming model, etc. will be considered.
- Write thesis Including problem definition, solution approach, SG kernels and their implementation, benchmark results, etc.
- Publish results

Overview of corner cases:

Illustration of 5G application challenges on a terminal device.



5G 1 basic TTI consisting of 1 Slot with 7 or 14 Symbols
4G 1 basic TTI has 2 slots with total of 14 Symbols